Amendments to the Specification:

Please replace the paragraph at page 1, lines 5-8 with the following rewritten paragraph:

--The present ~~invention generally~~ disclosure relates generally to phase locked loops (hereinafter, referred to as 'PLL'), and more specifically, to a PLL having a controller for dividing values of a voltage ~~control~~ controlled oscillator (hereinafter, referred to as 'VCO') in all [[the]] frequency [[band]] bandwidths.--

Please replace the section heading at page 1, line 10 with the following rewritten section heading:

~~--Description of the Related Art~~ Background--

Please replace the paragraph at page 1, lines 11-12 with the following rewritten paragraph:

--FIG. 1 is a block diagram illustrating a ~~general~~ conventional PLL having a program counter.--

Please replace the paragraph at page 2, line 9 with the following rewritten paragraph:

--FIG. 2 is a block diagram illustrating a ~~general~~ conventional PLL having a prescaler.--

Please replace the paragraph at page 4, lines 20-23 with the following rewritten paragraph:

~~--Accordingly,~~ In accordance with the present ~~invention has an object to operate~~ disclosure, a VCO may operate linearly at various frequencies by overlapping several VCOs and using a control circuit for selecting one VCO operating at a desired frequency. ~~outputted from the several VCOs, thereby satisfying characteristics of design in a on-chip PLL.--~~

Please replace the paragraph at page 4, lines 24-25 with the following rewritten paragraph:

--~~There is provided a~~ A PLL ~~comprising~~ includes a phase comparator, a filter, a VCO, a prescaler, a program counter, a swallow counter, [[and]] a controller[[.]], and a control signal generator.--

Please replace the paragraph beginning at page 4, line 26 and ending at page 5, line 4 with the following rewritten paragraph:

--The phase comparator compares a reference frequency of an external clock signal with a comparison frequency of a comparison clock signal. The filter filters an output signal from the phase comparator. The VCO generates clock signal [[of]] having a frequency proportional to a DC signal from the filter. The prescaler selectively divides the output clock signal from the VCO by using at least two ~~or more~~ division ratios. The program counter divides an output signal from the prescaler [[with]] by a ~~predetermined~~ division ratio to output the comparison clock signal having the comparison frequency. The swallow counter selects the division ratio of the prescaler. The controller controls the prescaler by using output signals from the program counter and the swallow counter. The control signal generator outputs a control signal to control frequency division of the VCO by using set points of the prescaler, the swallow counter and the program counter.--

Please replace the paragraph at page 5, lines 9-10 with the following rewritten paragraph:

--FIG. 1 is a block diagram illustrating a ~~general~~ conventional PLL having a program counter.--

Please replace the paragraph at page 5, line 11 with the following rewritten paragraph:

--FIG. 2 is a block diagram illustrating a ~~general~~ conventional PLL having a prescaler.--

Please replace the paragraph at page 5, lines 14-15 with the following rewritten paragraph:

--FIG. 4 is a block diagram illustrating a PLL having a swallow counter according to the present ~~invention~~ disclosure.--

Please replace the paragraph at page 5, lines 18-19 with the following rewritten paragraph:

--FIG. 6 is a circuit diagram illustrating a control bit generator of the ~~disclosed~~ VCO according to the present ~~invention~~ disclosure.--

Please replace the section heading at page 5, lines 21-22 with the following rewritten section heading:

--DETAILED DESCRIPTION ~~OF THE PRESENTLY PREFERRED EMBODIMENTS~~--

Please replace the paragraph at page 5, lines 23-24 with the following rewritten paragraph:

--The present ~~invention~~ disclosure will be described in detail with reference to the accompanying drawings.--

Please replace the paragraph at page 5, lines 25-26 with the following rewritten paragraph:

--FIG. 4 is a block diagram illustrating a PLL having a swallow counter according to the present ~~invention~~ disclosure.--

Please replace the paragraph beginning at page 5, line 27 and ending at page 6, line 4 with the following rewritten paragraph:

~~--The disclosed~~ A PLL in accordance with the present disclosure ~~comprises~~ includes a phase comparator 31, a low pass filter 32, a VCO 33, a dual modulus prescaler 34, a program counter 35, a swallow counter 36, a controller 37 and a control bit generator 38. The phase comparator 31 compares a reference frequency fr of an external clock signal ECLK with a comparison frequency fp of a comparison clock signal PCLK. The VCO 33 generates an internal clock signal Iclk [[of]] having a frequency proportional to a DC signal from the low pass filter 32. The dual modulus prescaler 34 divides an internal clock signal ICLK [[into]] by division ratios 1/M and 1/(M+1). The program counter 35 divides an output clock signal from the prescaler 34 [[into]] by a division ratio 1/N. The swallow counter 36 divides an output clock signal from the prescaler 34 [[into]] by a division ratio 1/A. The controller 37 controls the prescaler 34 by using output signals from the program counter 35 and the

swallow counter 36. The control bit generator 38 generates a control bit CB for controlling the VCO 33.--

Please replace the paragraph at page 6, lines 18-27 with the following rewritten paragraph:

--When the frequency division VCO 33 is used, values of N and A are used as control input values. In other words, if the control bit generator 38 uses the values of N and A as control input values, the frequency division VCO 33 can be controlled. ~~Here, it is preferable that the~~ The control bit generator 38 generates the control bit CB for controlling the frequency division VCO 33 by using the set point A of the swallow counter 36, the set point N of the program counter 35, and the set point M of the prescaler 34. However, since the control bit CB becomes larger and the circuit of the control bit generator 38 becomes complicated, the control bit generator 38 for generating the control bit CB is explained herein by using the set point N of the program counter 35 and the set point A of the swallow counter 36.--

Please replace the paragraph at page 7, lines 1-2 with the following rewritten paragraph:

--FIG. 5 is a graph illustrating an example of the frequency range of [[a]] an RF2 VCO and the division of regions.--

Please replace the paragraph at page 8, lines 3-4 with the following rewritten paragraph:

--FIG. 6 is a circuit diagram illustrating a control bit generator 38 of the ~~disclosed~~ VCO 33 according to the present ~~invention~~ disclosure.--

Please replace the paragraph beginning at page 8, line 5 and ending at page 9, line 7 with the following rewritten paragraph:

--The control bit generator 38 ~~comprises~~ includes: inverters INV1, INV2 and INV3[[,]]; NOR gates NOR1, NOR2, NOR3, NOR4, NOR5, NOR6, NOR7 and NOR8[[,]]; NAND gates ND1, ND2 and ND3[[,]]; and a D flip-flop 40. The inverters INV1 and INV2 invert[[s]] the division value A of the swallow counter 36. The inverter INV3 inverts the division value N of the program counter 34. The NOR gate NOR1 NORs output signals from

the inverters INV1 and INV2. The NAND gate ND1 NANDs an inverted output signal from NOR gate NOR1 and the division value A of the swallow counter 36. The NOR gate NOR2 NORs the division value A of the swallow counter 36 and an output signal from the inverter INV2. The NOR gate NOR3 NORs the division value A of the swallow counter 36 and an output signal from the inverter INV1. The NOR gate NOR4 NORs the division value A of the swallow counter 36 and an output signal from the inverter INV3. The NAND gate ND3 NANDs an inverted signal of the division value A of the swallow counter 36 and the division value of the program counter 34. The NOR gate NOR5 NORs an inverted output signal of the NAND gate ND2 and output signals from the NOR gates NOR2 and NOR3. The NOR gate NOR6 NORs an inverted output signal of the inverter INV3, the division value A of the swallow counter 36 and an output signal from the NOR gate NOR1. The NOR gate NOR7 NORs output signals from the NOR gate NOR3 and the inverter INV3. The NOR gate NOR8 NORs output signals from the NOR gate NOR1 and the inverter INV3. The D flip-flop 40 includes a reset input terminal R to receive the division value A of the swallow counter 36, a clock input terminal C to receive the output signal from the NAND gate ND3, and a data input terminal D to receive the output signal from the NOR gate NOR4. The control bit CB is generated by the NOR gates NOR5, NOR6, NOR7, NOR8 and the D flip-flop 40.--

Please replace the paragraph at page 9, lines 8-11 with the following rewritten paragraph:

--Most PLLs in the current market ~~comprise~~ include VCOs and filters installed outside. These external components have a great effect on cost and yield of products. Accordingly, since frequencies are pre-compensated automatically, the ~~embodiment of the whole~~ PLL can be simplified and compensated precisely.--

Please replace the paragraph at page 9, lines 12-16 with the following rewritten paragraph:

--As discussed ~~earlier,~~ above, in the disclosed PLL including the prescaler, frequencies can be pre-compensated automatically by using the control signal used in the PLL. As a result, a separate frequency compensation signal is not required. Additionally,

when the VCO is built [[in]] within the PLL, the ~~whole circuit of the~~ entire PLL circuit can be embodied [[into]] on a single chip.--

Please replace the paragraph at page 9, lines 17-22 with the following rewritten paragraph:

--While the ~~invention~~ disclosure is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and described in detail herein. However, it should be understood that the invention is not limited to the particular forms disclosed. Rather, the invention covers all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined in the appended claims.--